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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,737	07/09/2007	Atsuo Ishizuka	1982-0316PUS1	5298
2292 7590 10/07/2009 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				
EXAMINER PERRY, ANTHONY T				
ART UNIT		PAPER NUMBER		
2879				
NOTIFICATION DATE		DELIVERY MODE		
10/07/2009		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

# Office Action Summary

**Application No.**

10/594,737

**Applicant(s)**

ISHIZUKA ET AL.

**Examiner**

ANTHONY T. PERRY

**Art Unit**

2879

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 June 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/CDC)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_
- Paper No(s)/Mail Date \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masataka et al. (JP 10-339880) in view of Terao et al. (US 6,133,581).

Regarding claim 1, Masataka et al. disclose a display apparatus, comprising: a substrate (1); a first electrode group (3) made up of a plurality of electrode patterns (3+20) which are arranged adjacent to one another on the substrate (1), and extend in a first direction; a second electrode group (2) made up of a plurality of electrode patterns (2) which are arranged adjacent to one another on the substrate, and extend in a second direction which is different from the first direction; and a plurality of display elements which are each formed in correspondence to an intersection point of one electrode pattern among the first electrode group and one electrode pattern among the second electrode group, wherein at least the first electrode group includes a plurality of electrode patterns which are each connected to a drive circuit at one end, and are different in length from the one end to the other end, each of the plurality of electrode patterns has a lamination structure which has a first conductor (20) having a first sheet resistivity, and a second conductor (3) having a second sheet resistivity lower than the first sheet resistivity, each of the plurality of electrode patterns is provided with a higher resistance region where the second conductor (3) is removed, and the length of the higher resistance region is changed

according to the length of the electrode pattern for each of said plurality of electrode patterns (for example, see paragraph 0060), wherein, on the substrate, a display region (A) where the plurality of electrode patterns extend in parallel with one another at a first spacing, a terminal region (7) where the one ends of the plurality of electrode patterns in the display region are arranged at a second smaller spacing, and a connection part where the plurality of electrode patterns in the display region (A) are respectively connected to the corresponding one ends in the terminal region (7) are provided (for example, see Figs. 1 and 2).

Masataka et al. do not specifically disclose an arrangement wherein the location of the first conductor pattern and second conductor pattern are mutually displaced. However, such an arrangement of the first conductor pattern (2a) with respect to the second conductor pattern (2b) is a known alternative to the arrangement disclosed by Masataka (for example, see Figs. 5, 6a, and 6b of the Terao et al. reference). Terao et al. state that the arrangement shown in 6b provides a method of reducing the resistance in the same manner as the arrangement shown in Fig. 5. It has been held that the selection of a known alternative involves only routine skills in the art. Thus, one having ordinary skills in the art at the time the invention was made would have reasonably contemplated providing the arrangement wherein the location of the first conductor pattern and second conductor pattern are mutually displaced, since the selection of known alternatives is considered within the skills of the art, as evidenced by Terao et al..

Regarding claim 2, Masataka et al. teach the electrode patterns longer in length have a resistance region of a shorter length compared to electrode patterns shorter in length.

Regarding claim 3, Masataka et al. teach the plurality of electrode patterns have substantially the same resistivity value from the one end to the other end (for example, see the abstract and paragraph 0060).

Regarding claim 4, Masataka et al. teach the display apparatus of claim 1, wherein, on the substrate (1), a display region (A) where the plurality of electrode patterns extend in parallel with one another at a first spacing, a terminal region (7) where the one ends of said plurality of electrode patterns in the display region (A) are arranged at a second smaller spacing, and a connection part where the plurality of electrode patterns in the display region (A) are respectively connected to the corresponding one ends in the terminal region (7) are provided, in the terminal region, in each of the electrode patterns, the second conductor is removed, and the higher resistance region is formed such that it is continued to the terminal region (7) in the connection region (for example, see Fig. 1).

Regarding claim 5, Masataka et al. teach the display apparatus of claim 4, wherein, in the display region (A), the plurality of electrode patterns constituting the first electrode group are repetitively formed in the second direction, among the plurality of electrode patterns, the length of the electrode pattern in the middle is the shortest, and the length of the electrode pattern is symmetrically increased from the electrode pattern in the middle toward both outside directions (for example, see Fig. 1).

Regarding claim 6, Masataka et al. teach the display apparatus of claim 5, wherein, in the connection region, the plurality of electrode patterns extend while maintaining the parallel relationship (for example, see Fig. 1).

Regarding claim 7, Masataka et al. teach the display apparatus of claim 5, wherein the higher resistance region has the greatest length at the electrode pattern in the middle, and the length of the higher resistance region is symmetrically reduced from the electrode pattern in the middle toward both outside directions (for example, see Fig. 1).

Regarding claim 8, Masataka et al. teach the length of the higher resistance region being reduced from the electrode pattern in the middle toward both outside directions, but does not specifically show the length of the higher resistance region being linearly reduced according to the distance from the electrode pattern in the middle. However, it is noted that the applicant's specific limitation of the relation of the region being linearly reduced, does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of choice, which a person of ordinary skill in the art would have found obvious to select any relation (linearly, stepwise, etc.) of the reduction of the higher resistance region as long as it is reduced from the center shorter electrode pattern towards both outside directions, such that the relation of the reduction in the higher resistance regions results in the electrode patterns being uniform is resistance.

Regarding claim 9, Masataka et al. show the length of the higher resistance region being stepwise reduced from the electrode pattern in the middle toward both outside directions according to the distance from the electrode pattern in the middle (for example, see Fig. 1).

Regarding claim 10, Masataka et al. teach the first conductor (20) is made up of a transparent oxide electrode material, and the second conductor (3) is made up of a metallic material (for example, see paragraph 0060).

Regarding claim 11, Masataka et al. do not specifically recite the second conductor being laminated on the first conductor. However, it has been held that rearranging of parts of an invention involves only routine skills in the art. Thus, it would have been obvious to one having ordinary skills in the art the time the invention was made to laminate the second conductor on the first conductor or vice versa, since rearrangement of parts of an invention is considered within the skills of the art.

Regarding claim 12, Masataka et al. teach the display apparatus of claim 1, wherein the second conductor (3) is embedded in the first conductor (20) (for example, see paragraph 0059 and Fig. 1).

Regarding claims 13, Masataka et al. teach the display apparatus of claim 1, wherein an electrode pattern in the second electrode group (2) is connected to another drive circuit, and an electrode pattern in the first electrode group (3) forms, with the electrode pattern in the second electrode group (2), a current path for the drive current flowing in a display element which is formed at the intersection point (for example, see Fig. 2).

Regarding claim 14, Masataka et al. disclose the display apparatus of claim 1 being a liquid crystal display apparatus. It is noted that the same technical problem (non-uniform resistance of electrode lines having different lengths), for which Masataka provides a solution, exists in other display apparatuses, including an organic EL display apparatus. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same configuration taught by Masataka et al. in order to provide a uniform resistance for the electrode patterns in an organic electroluminescent device.

Regarding claim 15, Masataka et al. do not specifically teach the second conductor partially overlapping the first conductor in the direction along the width of the electrode pattern. However, it is noted that the applicant's specific limitation of the second conductor overlapping the first conductor, does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of choice, which a person of ordinary skill in the art would have found obvious to select any relationship of the second conductor to the first conductor in the width direction (equal widths, the first conductor overlapping the second conductor, or the second conductor overlapping the first conductor) as long as the two conductors are electrically connected such that the first electrode patterns have a uniform resistance.

Regarding claim 16, Masataka et al. teach the display apparatus of claim 1, wherein the first conductor (20) is laminated on the second conductor (3) (for example, see paragraph 0059 and Fig. 1).

Regarding claim 17, Masataka et al. do not specifically teach the second conductor partially overlapping the first conductor in the direction along the width of the electrode pattern. However, it is noted that the applicant's specific limitation of the second conductor overlapping the first conductor, does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of choice, which a person of ordinary skill in the art would have found obvious to select any relationship of the second conductor to the first conductor in the width direction (equal widths, the first conductor overlapping the second conductor, or the second conductor overlapping the



first conductor) as long as the two conductors are electrically connected such that the first electrode patterns have a uniform resistance.

***Response to Arguments***

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Anthony Perry* whose telephone number is (571) 272-2459. The examiner can normally be reached between the hours of 9:00AM to 5:30PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. **The fax phone number for this Group is (571) 273-8300.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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